

FIG. 1

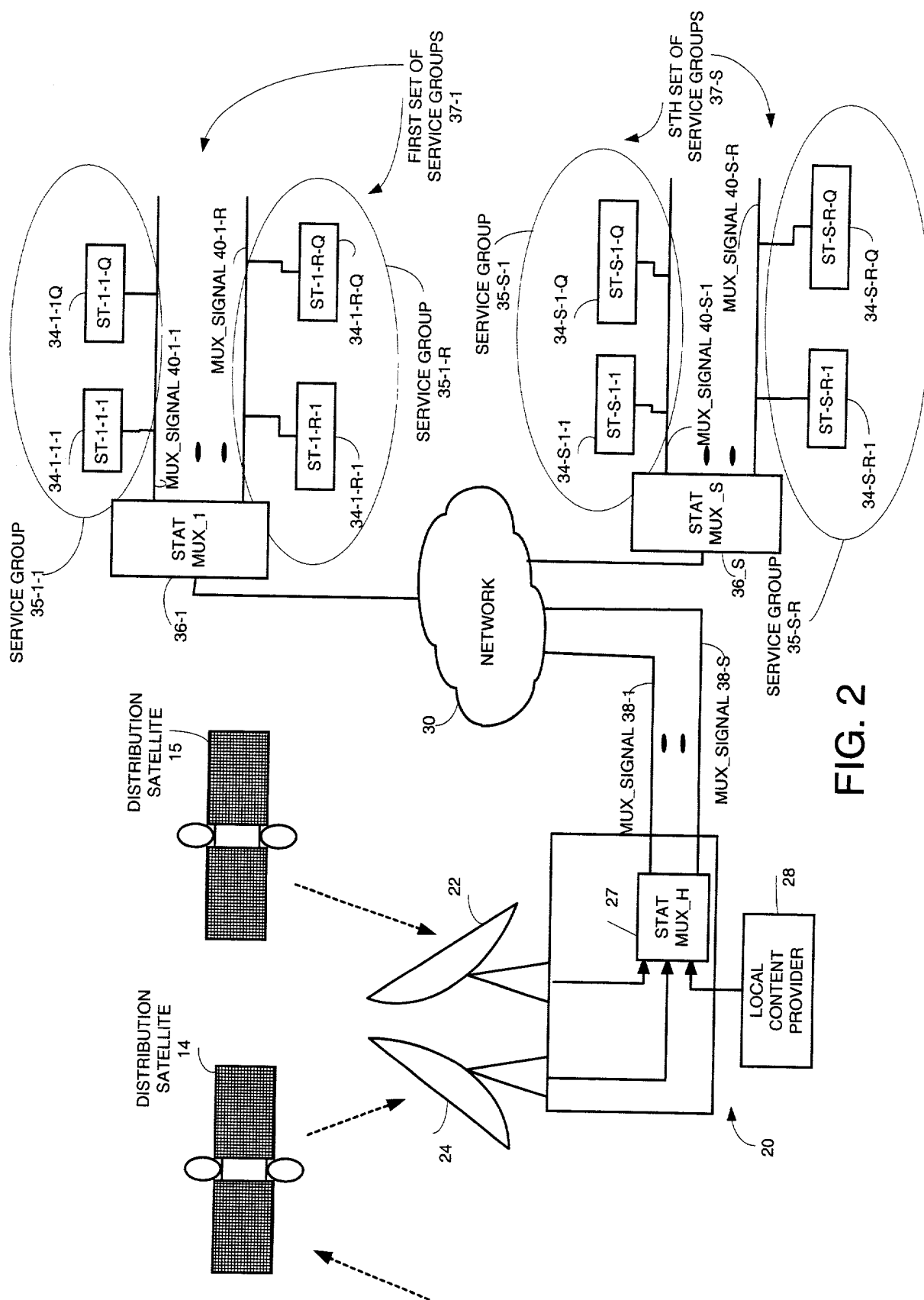


FIG. 2

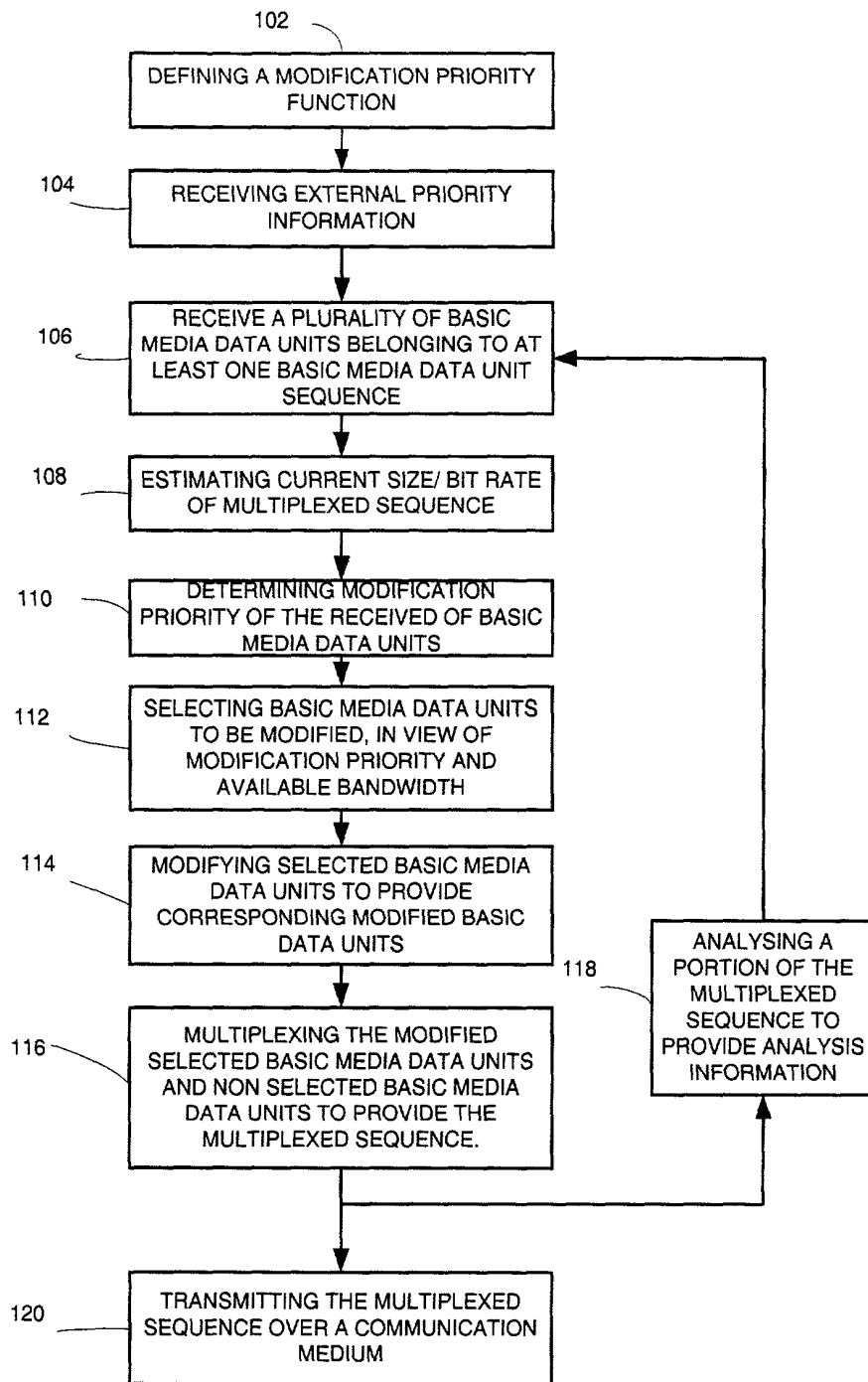
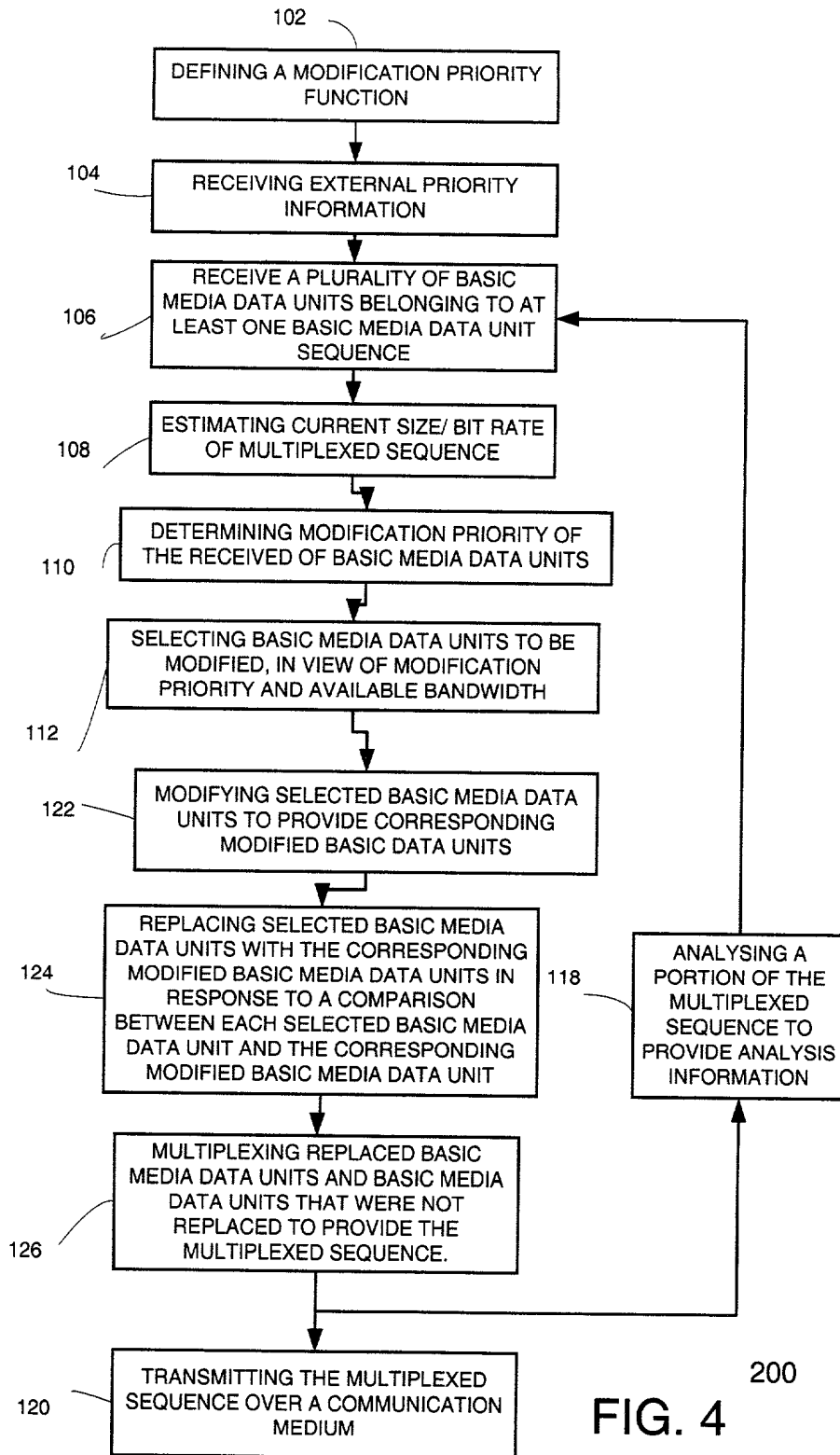


FIG. 3



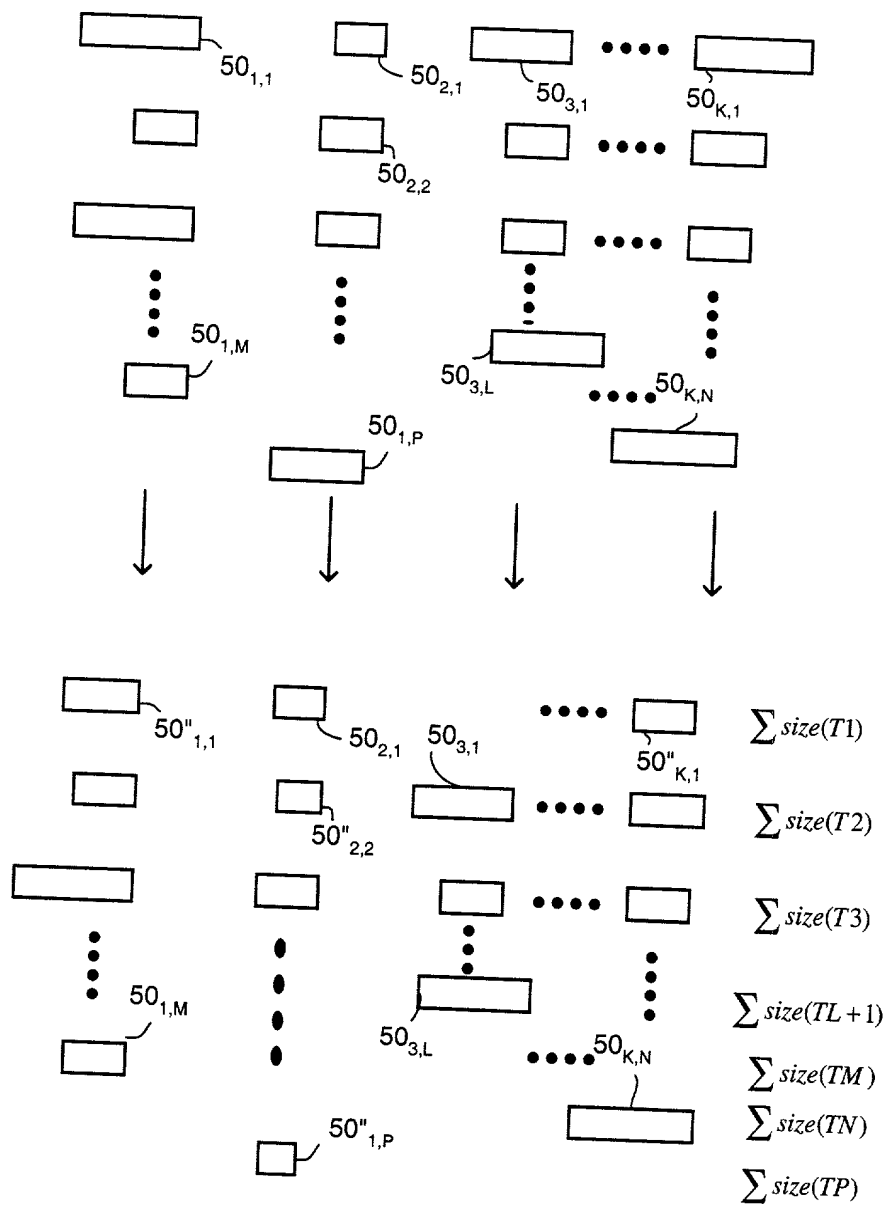


FIG. 5

FIG. 6 is a block diagram of a system 200 for simulating a packetizing output mux 7.

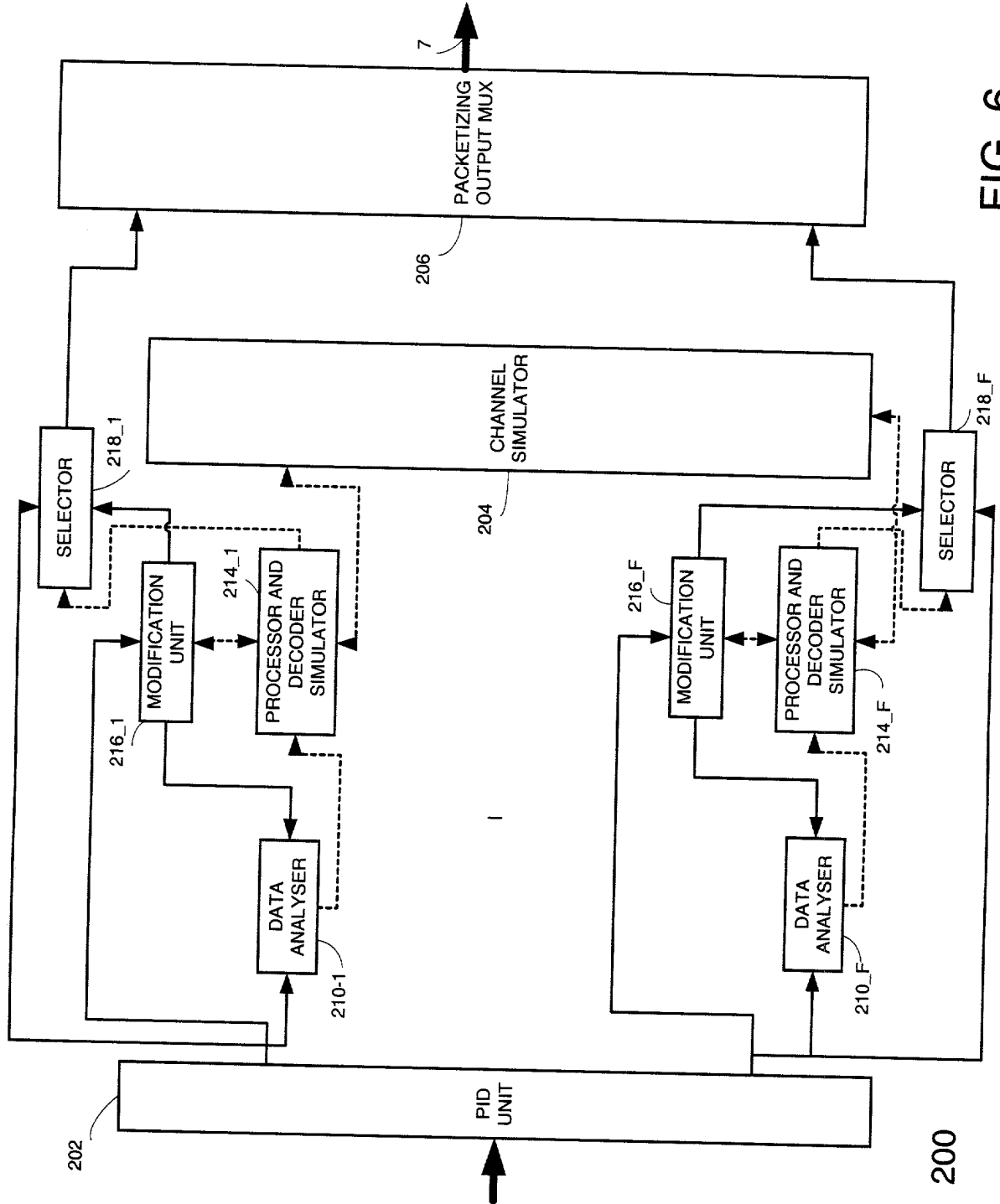


FIG. 6